Attorney Docket No. 10555-054

UNDER THE PATENT COOPERATION TREATY

Applicant:	Picometrix, Inc
Int'l Appl. No.:	PCT/US03/03323
Int'l Filing Date:	03 February 2003
Authorized Officer:	Minhloan T. Tran
For:	PLANAR AVALANCHE PHOTODIODE

RESPONSETO WRITTEN OPINION

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents, Attn: IPEA/US (703-305-3230) on February 25, 2004.

By Terry Wand
Terry Wand

Mail Stop PCT, Attn: IPEA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Written Opinion mailed December 30, 2003, for which the response period extends to February 29, 2004, please consider the following:

SUBSTITUTE SHEETS

IN THE CLAIMS:

The claims are being amended for clarity. No new matter is being added. Substitute sheets for those pages of the application which are being amended are enclosed herewith. The substitute sheets include pages 10 through 13 to replace pages 10 through

13 containing the claims. The substitute claims differ from the claims originally on file as follows:

Original claims 1-3, 5-11, 13-16, 19-21, 23, 25, 26, 29, and 30 have been amended. Original claims 17, 18, 22 and 24 have been cancelled. Substitute claims 1-16 maintain their original numbering. In view of the cancellation of claims 17, 18, 22 and 24, original claims 19- 21, 23, 25-27, 29, and 30 have been respectively renumbered as claims 17-25. Please note that the application was filed without a claim 28. This typographical error has been corrected by the renumbering of the claims.

Specifically, amended claims 1, 9, and 17 require a photodiode having a semiconductor layer with a p-type diffusion region and a semiconductor absorption layer disposed between a semiconductor multiplication layer and the semiconductor layer with the p-type diffusion region. Moreover, amended claims 1, 9, and 17 require the p-type diffusion layer to have a smaller area than the semiconductor layer, and claim 17 also includes the limitation "wherein the photodiode has a low field region near the p-type semiconductor layer and a low capacitance."

STATEMENT UNDER RULE 66.2(a)(ii)

The Authorized Officer has stated that claims 1, 4, 9, 12, 17, 19, and 22 would not meet the novelty requirement stipulated in Article 33(2) PCT, and that claims 1, 4-9, 12-19, and 22-27 would not meet the inventive step requirement under Article 33(3) PCT. In particular, the Officer contends that original independent claims 1, 9, 17, and 19 are anticipated by U.S Patent No. 4,849,916 to Yasuda et al. and are obvious in view of U.S. Patent No. 5,552,629 to Watanabe.

In response, Applicants have cancelled claims 17, 18, 22 and 24 and have amended original claims 1-3, 5-11, 13-16, 19-21, 23, 25, 26, 29, and 30. Substitute claims 1 through 16 maintain their original numbering and original claims 19-21, 23, 25-27, 29, and 30 have been respectively renumbered as claims 17-25.

As amended, claims 1, 9, and 17 each requires a semiconductor layer with a p-type diffusion layer disposed adjacent to a p-type contact layer and the p-type diffusion layer have a smaller area than that of the semiconductor layer. Claims 1, 9, and 17 also require an absorption layer disposed between the p-type diffusion layer and a multiplication layer. The present invention provides a photodiode with a structure that is reversed from conventional avalanche photodiodes since electrons, rather than holes are being avalanched in the multiplication layer. This structural inversion allows the low field region in the absorption region to be at the top of the device rather than in the high field avalanche region as in conventional avalanche photodiodes.

Yasuda discusses a photodiode with a p-type region (8) in an n-type semiconductor layer (16) and a multiplication layer (16) disposed between an absorption layer (3) and the p-type region (8). Therefore, Yasuda does not teach an absorption layer disposed between a p-type diffusion layer and a multiplication layer, as required by amended claims 1, 9, and 17.

Watanabe discusses a photodiode that includes a p-type semiconductor layer (56) with an n-type diffusion layer (58) and a multiplication layer (55) disposed between an absorption layer (53) and the n-type diffusion layer (58). Thus, Watanabe does not describe a photodiode with an absorption layer disposed between a p-type diffusion layer and a multiplication layer, as required by amended claims 1, 9, and 17. Indeed, Watanabe

fails to appreciate the advantages associated with placing the absorption layer between the p-type diffusion layer and the multiplication layer. Absent an appreciation of these advantages, there is no suggestion of a photodiodes with the structure recited in amended claims 1, 9, and 17.

Accordingly, since Yasuda and Watanabe neither teaches nor suggests a photodiode with the structure recited in amended claims 1, 9, and 17, amended claims 1, 9, and 17 meet the novelty and inventive step requirements. Because the new claims 2-8, 10-16, and 18-25 depend, directly or indirectly, from amended claims 1, 9, or 17, the reasons amended claims 1, 9, and 17 meet the novelty and inventive step requirements apply as well to the dependent claims.

CONCLUSION

In view of the preceding amendments and remarks, the Applicants respectfully submit that the specification and drawings are in order and that all of the claims are now in condition for allowance.

Respectfully submitted,

Date: Feb. 25, 2004

By: _____
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CLAIMS

What is claimed is:

1. A planar avalanche photodiode comprising:

an n-type semiconductor layer defining a contact area;

a semiconductor layer having a p-type diffusion region, the p-type diffusion region having a smaller area than the semiconductor layer;

a semiconductor multiplication layer;

a semiconductor absorption layer; and

a p-type contact layer;

wherein the p-type diffusion region is disposed directly adjacent to the p-type contact layer, and the semiconductor absorption layer is disposed between the semiconductor multiplication layer and the semiconductor layer with the p-type diffusion region.

2. The planar avalanche photodiode of claim 1 further comprising at least one grading layer disposed adjacent to the semiconductor absorption layer.

3. The planar avalanche photodiode of claim 1 further comprising a p-type semiconductor charge control layer disposed adjacent to the semiconductor multiplication layer.

4. The planar avalanche photodiode of claim 1 further ~~comprising at~~ least one n-type contact layer.

5. The planar avalanche photodiode of claim 1 wherein the n-type semiconductor layer is InAlAs.

6. The planar avalanche photodiode of claim 1 wherein the semiconductor layer with the p-type diffusion layer is InAlAs.

7. The planar avalanche photodiode of claim 1 wherein the semiconductor multiplication layer is InAlAs.

8. The planar avalanche photodiode of claim 1 wherein the semiconductor absorption layer is InGaAs.

9. A method of fabricating a planar avalanche photodiode comprising the following steps:

providing an n-type semiconductor layer defining a contact area;

depositing a semiconductor layer;

depositing a semiconductor multiplication layer;

depositing a semiconductor absorption layer;

depositing a p-type contact layer; and

diffusing a p-type diffusion region having a smaller area than the semiconductor layer directly adjacent to the p-type contact layer, thereby decreasing the capacitance of the planar avalanche photodiode.

10. The method of claim 9 further comprising the step of depositing at least one grading layer adjacent to the semiconductor absorption layer.

11. The method of claim 9 further comprising the step of depositing a p-type semiconductor charge control layer adjacent to the semiconductor multiplication layer.

12. The method of claim 9 further comprising the step of depositing at least one n-type contact layer.

13. The method of claim 9 wherein the n-type semiconductor layer is InAlAs.

14. The method of claim 9 wherein the deposited semiconductor layer is InAlAs.

15. The method of claim 9 wherein the semiconductor multiplication layer is InAlAs.

16. The method of claim 9 wherein the semiconductor absorption layer is InGaAs.

17. A planar avalanche photodiode comprising:

an n-type semiconductor layer defining a contact area;

a semiconductor multiplication layer;

a semiconductor absorption layer, the semiconductor multiplication layer being disposed between the first n-type semiconductor layer and the semiconductor absorption layer; and

a p-type semiconductor contact layer having a smaller area than the absorption layer, the semiconductor absorption layer being disposed between the semiconductor multiplication layer and the p-type semiconductor contact layer,

wherein the photodiode has a low field region near the p-type semiconductor contact layer and a low capacitance.

18. The planar avalanche photodiode of claim 17 further comprising at least one grading layer disposed adjacent to the semiconductor absorption layer.

19. The planar avalanche photodiode of claim 17 further comprising a p-type semiconductor charge control layer disposed adjacent to the semiconductor multiplication layer.

20. The planar avalanche photodiode of claim 17 wherein the n-type semiconductor layer is InAlAs.

21. The planar avalanche photodiode of claim 17 wherein the semiconductor multiplication layer is InAlAs.

22. The planar avalanche photodiode of claim 17 wherein the semiconductor absorption layer is InGaAs.

23. The planar avalanche photodiode of claim 17 wherein the p-type semiconductor contact layer is InAlAs.

24. The planar avalanche photodiode of the claim 17 further comprising a passivated region including a semiconductor layer disposed between the p-type contact layer and the semiconductor absorption layer.

25. The planar avalanche photodiode of claim 24 wherein the passivated region includes a portion of a first grading layer and a portion of the semiconductor absorption and multiplication layers.